

## **REMARKS**

Reconsideration of the above-identified Application is respectfully requested. Claims 1-30 are in the case. Claim 23 has been amended.

Regarding the objection to Claim 23, this claim has been amended in accordance with the Examiner's kind suggestion, thereby overcoming the ground for this objection. Wherefore reconsideration and withdrawal of this objection are respectfully requested.

Regarding the rejection of Claims 1-30 under 35 U.S.C. § 102(b) as allegedly being anticipated by Stephenson, Jr. et al., this rejection is respectfully traversed. Independent Claim 1 recites a bit-rate detection circuit including logic circuitry responsively coupled to shift registers providing an output signal indicative of the data frequency of data serially shifted into the shift registers. Independent Claim 16 recites a data transceiver including logic circuitry responsively coupled to a receiver circuit determining a data rate of data received by the data receiver. Independent Claim 21 recites a method of detecting a bit-rate of data incoming to a receiver including the step of analyzing data at a plurality of nodes between a plurality of shift registers to determine the bit rate of the incoming data. Independent Claim 28 recites a bit-rate detection circuit including logic circuitry responsively coupled to a plurality of shift registers providing an output indicative of the data rate. Common to all of these independent claims is an element or step for determining a bit rate or data rate.

The patent to Stephenson, Jr. et al. apparently relates to a parallel frame synchronization circuit which converts a high-speed serial bit stream into a lower speed parallel stream of multi-bit words, including a circuit comparing the multi-bit words for determining the location within the bit stream of frame synchronization information. Nowhere in this reference is any mention made of any circuit, method or any other means for determining a data rate or bit rate. Indeed, the embodiments disclosed in this reference assume that the incoming data is at a fixed, predetermined rate. For example, for an embodiment adapted

to operate in accordance with the SONET STS-3 standard, the frequency is assumed to be that set by that standard, namely 155.52 megabits per second (see Column 5, lines 26-29). Thus, there is no need for any means for determining a bit rate, and therefore no suggestion or motivation for such determination.

The other art of record is even less relevant.

Therefore, for the above reasons it is respectfully submitted that independent Claims 1, 16, 21 and 28 are neither anticipated nor suggested by the reference to Stephenson, Jr. et al., nor by any of the art of record, whether considered alone or in any combination, and that these claims are allowable over all of the art of record. The other claims subject to this rejection depend, directly or indirectly from one of Claims 1, 16, 21 and 28, and so those claims are allowable as well for the same reasons, as well as for the additional limitations found therein. Wherefore reconsideration and withdrawal of this rejection are respectfully requested.

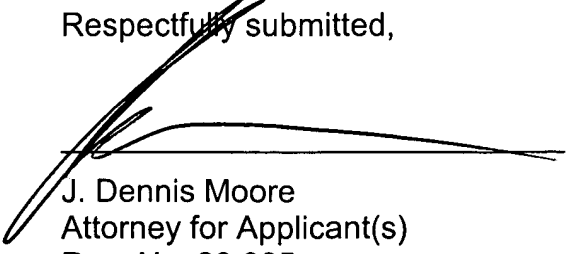
It is respectfully submitted that the claims recite the patentably distinguishing features of the invention and that, taken together with the above remarks, the present application is now in proper form for allowance. Reconsideration of the application, as amended, and allowance of the claims are requested at an early date.

While it is believed that the instant amendment places the application in condition for allowance, should the Examiner have any further comments or suggestions, it is respectfully requested that the Examiner contact the undersigned in order to expeditiously resolve any outstanding issues.

To the extent necessary, the Applicants petition for an Extension of Time under 37 C.F.R. §1.136. Please charge any fees in connection with the filing of this paper, including extension of time fees to the Deposit Account No. 20-0668

of Texas Instruments Incorporated.

Respectfully submitted,



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